

DOCKET NO. CML00320CR

REMARKS

In an Office Action mailed January 25, 2005, pending claims 1-16 were examined and rejected. In response, Applicants have amended claims 3, 5, 7 and 9 while requesting entrance of a previously filed preliminary amendment, and respectfully request the allowance of the application. No additional fees are owed as a result of the claim amendments.

Claims 1-16 were rejected under 35 U.S.C. 112, first paragraph. One of the bases for this rejection clearly indicates that the preliminary amendment filed by Applicants on July 27, 2004 using the 37 C.F.R. 1.8 facsimile certificate rule was not considered by the Examiner. Typographical errors in the specification were corrected with that amendment. In particular, in paragraph [0027] at the fourth line of the paragraph, a typo was corrected to make clear that a resultant magnetic moment vector 86 as represented by ΔM_{86} is equal to the magnetic moment vector M_{84} minus magnetic moment vector M_{82} . This relationship is again stated in the immediately following line as equal numerators wherein $(M_{84}-M_{82})$ is equated to ΔM_{86} . Thus correction of this typographical error adds no new matter to the specification and makes consistent an obvious inadvertent error in paragraph [0027]. The July 27, 2004 preliminary amendment also corrects another obvious typographical error on page 13 wherein the difference between R_{high} and R_{low} was inadvertently typed as a "square" R rather than a "delta" R in the expressed equation. Correction of this obvious error has previously been requested. With correction of these typographical errors in addition to typographical errors noted in paragraph [0050] of the previously filed preliminary amendment, Applicants request withdrawal of the stated rejection.

Claim 3 was also rejected under 35 U.S.C. 112, first paragraph, for being in a single means claim format. Claim 3 is amended to recite two steps, rather

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than a single step. Therefore, reconsideration and withdrawal of the rejection of claim 3 is respectfully requested.

Claims 1-16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland (U.S. Patent 6,567,304). Kleveland discloses a memory that can store two-bits per cell or multiple bits depending upon an amount of reduction of program/erase disturb voltage. The rejected claims are not reciting just the storage of two bits per memory cell. Rather, claims 1-16 recite a method of programming a memory cell and switching a magnetoresistive memory device by toggling the logic state of memory bits. There is no toggling operation taught or suggested by Kleveland. As described at Col. 3, lines 45 thru Col. 4, line 5, the Kleveland memory is programmed by using one or more pulses of predetermined voltage to put charge in a gate oxide or gate electrode by hot electron injection. Therefore, a certain charge is programmed into a portion of the memory cell structure of the Kleveland memory. Kleveland does not teach or suggest "toggling the logic state of the two bits" as recited in independent claim 1. Kleveland does not teach or suggest "toggling a logic state of a first of the two bits; and toggling a logic state of a second of the two bits independently of toggling the logic state of the first of the two bits" as recited in independent claim 3, as amended herein. Kleveland does not teach or suggest "deciding on one of or both of the steps comprising: applying current to each of the conductors, thereby toggling the logic state of the two bits; and applying a smaller current to each of the conductors, thereby toggling the logic state of only one of the bits." as recited in independent claim 5, as amended herein. The Kleveland memory functions by being programmed with a program voltage and then erased to a predetermined value with an erase voltage prior to again being programmed with the program voltage. Kleveland does not teach or suggest "programming the first bit to switch a state of the first bit by applying the second current to the second conductor and a third current to the first conductor, the third current being less in magnitude than the first current; and programming the second bit to switch a state of the second bit by applying the

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first current to the first conductor and a fourth current to the second conductor, the fourth current being less in magnitude than the second current." as recited in independent claim 9, as amended herein. The Kleveland memory is programmed with a voltage, and is not programmed by currents on conductors as recited and having predetermined relationships as recited in order to switch bit states as recited. Kleveland does not teach or suggest a magnetoresistive device having magnetic regions with magnetic moment vectors as recited in independent claim 11. Kleveland discloses a conventional floating gate memory structure in Fig. 1A therein and the functional operation of the Kleveland memory is considerably different from the method and structure recited in independent claim 11.

Applicants have considered the remaining made of record but not relied upon. Both Nahas (U.S. Patent 6,842,365) and Subramanian (U.S. Patent 6,714,440) relate to magnetoresistive memories or MRAM. However, there is one bit per cell in each MRAM cell in each reference and neither document teaches having two bits per cell in a magnetoresistive memory cell. Conley et al. (U.S. Patent 6,580,638) recites a Flash EEPROM in which simultaneous programming and storage of data may occur. The Conley et al. memory, like the Kleveland memory does not disclose or suggest magnetoresistive memory. By separate cover letter Applicants are submitting an Information Disclosure Statement and associated fee. The three U.S. patents which are referenced in the Background section of the application are listed in order to be formally considered since none of those patents were officially made of record in the Office Action. The associated fee authorization and cover letter accompany this response.

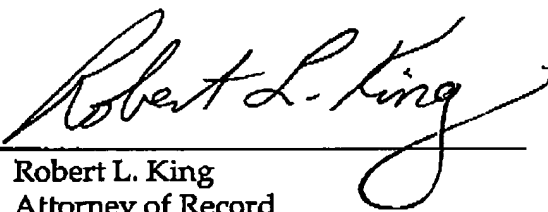
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Applicants thank the Examiner for the efforts expended on this application and respectfully request the allowance of claims 1-16.

Respectfully submitted,

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